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| APPLICATION NO. | FILING DATE | FIRST NAMED INVENTOR | ATTORNEY DOCKET NO. | CONFIRMATION NO. |
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| 10/533,291 | 02/07/2006 | Paul Colfer | 200316610-2 | 6028 |
| 22879 | 7590 | 07/19/2007 | | |
| HEWLETT PACKARD COMPANY | | | EXAMINER | |
| P O BOX 272400, 3404 E. HARMONY ROAD | | | HO, ANTHONY | |
| INTELLECTUAL PROPERTY ADMINISTRATION | | | | |
| FORT COLLINS, CO 80527-2400 | | | ART UNIT | PAPER NUMBER |
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| | | | 07/19/2007 | PAPER |

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

| | | |
|------------------------------|------------------------|---------------------|
| Office Action Summary | Application No. | Applicant(s) |
| | 10/533,291 | COLFER ET AL. |
| | Examiner | Art Unit |
| | Anthony Ho | 2815 |

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --
Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) Responsive to communication(s) filed on 17 May 2007.
- 2a) This action is FINAL. 2b) This action is non-final.
- 3) Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) Claim(s) 1-20,22-30,63,64,68,71 and 74-88 is/are pending in the application.
- 4a) Of the above claim(s) 76-88 is/are withdrawn from consideration.
- 5) Claim(s) _____ is/are allowed.
- 6) Claim(s) 1-20,22-30,63,64,68,71,74 and 75 is/are rejected.
- 7) Claim(s) _____ is/are objected to.
- 8) Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) The specification is objected to by the Examiner.
- 10) The drawing(s) filed on 29 April 2005 is/are: a) accepted or b) objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) All b) Some * c) None of:
 1. Certified copies of the priority documents have been received.
 2. Certified copies of the priority documents have been received in Application No. _____.
 3. Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- | | |
|--|---|
| 1) <input checked="" type="checkbox"/> Notice of References Cited (PTO-892) | 4) <input type="checkbox"/> Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948) | 5) <input type="checkbox"/> Notice of Informal Patent Application |
| 3) <input checked="" type="checkbox"/> Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date <u>4/29/2005</u> . | 6) <input type="checkbox"/> Other: _____ |

DETAILED ACTION

Election/Restrictions

Applicant's election without traverse of claims 1-20, 22-30, 63-64, 68, 71, and 74-75 in the reply filed on May 17, 2007 is acknowledged.

Accordingly, claims 76-88 are withdrawn from further consideration pursuant to 37 CFR 1.142(b) as being drawn to a nonelected invention, there being no allowable generic or linking claim. Election was made **without** traverse in the reply filed on May 17, 2007.

Priority

Receipt is acknowledged of papers submitted under 35 U.S.C. 119(a)-(d), which papers have been placed of record in the file.

Information Disclosure Statement

The information disclosure statement (IDS) submitted on April 29, 2005 in compliance with the provisions of 37 CFR 1.97. Accordingly, the information disclosure statement is being considered by the examiner.

Drawings

New corrected drawings in compliance with 37 CFR 1.121(d) are required in this application because most of the drawings such as Figure 16 and after are of very poor quality and better drawings are needed for better understanding of application.

Applicant is advised to employ the services of a competent patent draftsperson outside the Office, as the U.S. Patent and Trademark Office no longer prepares new drawings.

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The corrected drawings are required in reply to the Office action to avoid abandonment of the application. The requirement for corrected drawings will not be held in abeyance.

Claim Objections

Claims 2-20, 22-30, 63-64, 68, 71, and 74-75 are objected to because of the following informalities: The claims contain grammar mistakes and English spelling need to be corrected to American spelling such as "recrystallise" need to be "recrystallize". Appropriate correction is required.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 1-20, 22-30, 63-64, 68, 71, and 74-75 are rejected under 35 U.S.C. 102(b) as anticipated by or, in the alternative, under 35 U.S.C. 103(a) as obvious over Yudasaka et al (EP 1085578).

In re claims 1-3, Yudasaka et al discloses a method of manufacturing an electronic component comprising at least one n- or p-doped portion, comprising the steps of: co-depositing inorganic semi-conducting nanoparticles and dopant on a substrate, the

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nanoparticles comprising a group four element such as silicon or germanium; fusing the nanoparticles by heating to form a continuous layer; and subsequently; recrystallizing the layer (paragraph 0004; paragraph 0045 – paragraph 0066).

In re claims 4-6, Yudasaka et al discloses the step of fusing and/or recrystallizing is carried out in a reducing atmosphere (paragraph 0065).

In re claims 7-10, Yudasaka et al discloses the step of heating using laser pulses and cooling (paragraph 0045 – paragraph 00070).

In re claims 11-13, Yudasaka et al discloses the nanoparticles are deposited in a suspension of a carrier fluid (paragraph 0069 – paragraph 0074).

In re claims 14-18, Yudasaka et al discloses the different printing processes (paragraph 0045 – paragraph 0075).

In re claims 19-20, Yudasaka et al discloses the electronic component is a transistor, capacitor, or a diode (Figure 5; Figure 6; Figure 7).

In re claims 22-26, Yudasaka et al discloses a method of manufacturing an electronic component comprising at least one n- or p-doped portion, comprising the steps of: co-depositing discrete nanoparticles of semi-conducting material with a dopant on a

substrate; fusing the nanoparticles with one or more first laser pulses to form a continuous layer; and subsequently; recrystallizing the continuous layer (paragraph 0004; paragraph 0045 – paragraph 0075).

In re claims 27-29, Yudasaka et al discloses the step of fusing and/or recrystallizing is carried out in a reducing atmosphere (paragraph 0065).

In re claim 30, Yudasaka et al discloses the electronic component is a transistor, capacitor, or a diode (Figure 5; Figure 6; Figure 7).

In re claims 63-64 and 68, Yudasaka et al discloses both a first semiconducting material and a second semiconducting material (paragraph 0045 – paragraph 0070; Example 1).

In re claim 71, Yudasaka et al discloses depositing nanoparticles on a further substrate, causing the nanoparticles to fuse and recrystallise to form a recrystallized film or layer (paragraph 0045 – paragraph 0070; Example 1).

In re claims 74-75, Yudasaka et al discloses a component using the above method (Example 1; Figure 5, Figure 6, Figure 7).

Claims 1-20, 22-30, 63-64, 68, 71, and 74-75 are rejected under 35 U.S.C. 102(b) as anticipated by or, in the alternative, under 35 U.S.C. 103(a) as obvious

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over Furusawa et al (WO 00/59044 – US Patent 6,518,087 is patent family member used for citation purposes).

In re claims 1-3, Furusawa et al discloses a method of manufacturing an electronic component comprising at least one n- or p-doped portion, comprising the steps of: co-depositing inorganic semi-conducting nanoparticles and dopant on a substrate, the nanoparticles comprising a group four element such as silicon or germanium; fusing the nanoparticles by heating to form a continuous layer; and subsequently; recrystallizing the layer (column 9 – column 12).

In re claims 4-6, Furusawa et al discloses the step of fusing and/or recrystallizing is carried out in a reducing atmosphere (column 9 – column 12).

In re claims 7-10, Furusawa et al discloses the step of heating using laser pulses and cooling (column 9 – column 12).

In re claims 11-13, Furusawa et al discloses the nanoparticles are deposited in a suspension of a carrier fluid (column 9 – column 12).

In re claims 14-18, Furusawa et al discloses the different printing processes (column 9 – column 12).

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In re claims 19-20, Furusawa et al discloses the electronic component is a transistor, capacitor, or a diode (Figure 3; Figure 4; Figure 5).

In re claims 22-26, Furusawa et al discloses a method of manufacturing an electronic component comprising at least one n- or p-doped portion, comprising the steps of: co-depositing discrete nanoparticles of semi-conducting material with a dopant on a substrate; fusing the nanoparticles with one or more first laser pulses to form a continuous layer; and subsequently; recrystallizing the continuous layer (column 9 – column 12).

In re claims 27-29, Furusawa et al discloses the step of fusing and/or recrystallizing is carried out in a reducing atmosphere (column 9 – column 12).

In re claim 30, Furusawa et al discloses the electronic component is a transistor, capacitor, or a diode (Figure 3; Figure 4; Figure 5).

In re claims 63-64 and 68, Furusawa et al discloses both a first semiconducting material and a second semiconducting material (column 9 – column 12; Example 1).

In re claim 71, Furusawa et al discloses depositing nanoparticles on a further substrate, causing the nanoparticles to fuse and recrystallise to form a recrystallized film or layer (column 9 – column 12; Example 1).

In re claims 74-75, Furusawa et al discloses a component using the above method (Example 1; Figure 3; Figure 4; Figure 5).

Claims 1-20, 22-30, 63-64, 68, 71, and 74-75 are rejected under 35 U.S.C. 102(b) as anticipated by or, in the alternative, under 35 U.S.C. 103(a) as obvious over Kamata et al (US Patent 6,086,945).

In re claims 1-3, Kamata et al discloses a method of manufacturing an electronic component comprising at least one n- or p-doped portion, comprising the steps of: co-depositing inorganic semi-conducting nanoparticles and dopant on a substrate, the nanoparticles comprising a group four element such as silicon or germanium; fusing the nanoparticles by heating to form a continuous layer; and subsequently; recrystallizing the layer (column 5 – column 11).

In re claims 4-6, Kamata et al discloses the step of fusing and/or recrystallizing is carried out in a reducing atmosphere (column 5 – column 11).

In re claims 7-10, Kamata et al discloses the step of heating using laser pulses and cooling (column 5 – column 11).

In re claims 11-13, Kamata et al discloses the nanoparticles are deposited in a suspension of a carrier fluid (column 5 – column 11).

In re claims 14-18, Kamata et al discloses the different printing processes (column 5 – column 11).

In re claims 19-20, Kamata et al discloses the electronic component is a transistor, capacitor, or a diode (Figure 4A; Figure 4B; Figure 13).

In re claims 22-26, Kamata et al discloses a method of manufacturing an electronic component comprising at least one n- or p-doped portion, comprising the steps of: co-depositing discrete nanoparticles of semi-conducting material with a dopant on a substrate; fusing the nanoparticles with one or more first laser pulses to form a continuous layer; and subsequently; recrystallizing the continuous layer (column 5 – column 11).

In re claims 27-29, Kamata et al discloses the step of fusing and/or recrystallizing is carried out in a reducing atmosphere (column 5 – column 11).

In re claim 30, Kamata et al discloses the electronic component is a transistor, capacitor, or a diode (Figure 4A; Figure 4B; Figure 13).

In re claims 63-64 and 68, Kamata et al discloses both a first semiconducting material and a second semiconducting material (column 5 – column 11).

In re claim 71, Kamata et al discloses depositing nanoparticles on a further substrate, causing the nanoparticles to fuse and recrystallise to form a recrystallized film or layer (column 5 – column 11).

In re claims 74-75, Kamata et al discloses a component using the above method (column 5 – column 11).

Conclusion

The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. Cordaro (US Patent 6,689,950) discloses paint solar cell and its fabrication. Beppu et al (US Patent 5,866,471) discloses method of forming semiconductor thin film and method of fabricating solar cell. Matsuki et al (US PUB 2001/0021760) discloses novel cyclosilane compound, and solution composition and process for forming a silicon film. Janowiecki et al (US Patent 4,003,770) discloses plasma spraying process for preparing polycrystalline solar cells. Shimoda et al (WO 00/59015 – US Patent 6,541,354 is patent family member) discloses method for forming silicon film. Yudasaka et al (US Patent 6,767,775) discloses method of manufacturing thin-film transistor.

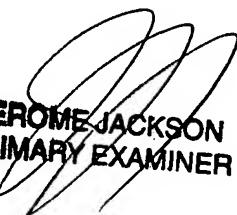
Any inquiry concerning this communication or earlier communications from the examiner should be directed to Anthony Ho whose telephone number is 571-270-1432. The examiner can normally be reached on M-Th: 8:30AM-7:00PM EST.

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If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Kenneth Parker can be reached on 571-272-2298. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

AH
June 6, 2007



JEROME JACKSON
PRIMARY EXAMINER